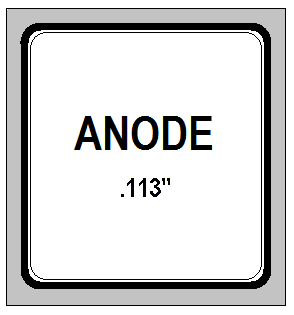
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**.130”**

**.130”**

**.104”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .104” X .104”**

**Backside Potential: CATHODE**

**Mask Ref: RC**

**APPROVED BY: DK DIE SIZE .130” X .130” DATE: 11/16/21**

**MFG: PPC / MICROSEMI THICKNESS .010” P/N: MURC1560**

**DG 10.1.2**

#### Rev B, 7/1